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GB 1467726
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(54) Improvements in or relating to information retrieval

(57) A small viewdata centre has a plurality of user ports 10 each of which provides an interface between the public switched telephone network 12 and a pair of serial highways 14, 15. System controllers 16 control communication between the user ports 10 and a data-base 18 via the serial highways 14, 15. The data-base 18 is linked to the highways 14, 15 by data-base controllers 19. Transmission along the highways 14, 15 is based on a high level data link control protocol which gives bit and frame synchronisation and a fixed protocol for the formation of messages. A feature of each user port 10 is a circuit for resolving clashes when two or more ports try to gain access to the highways simultaneously.

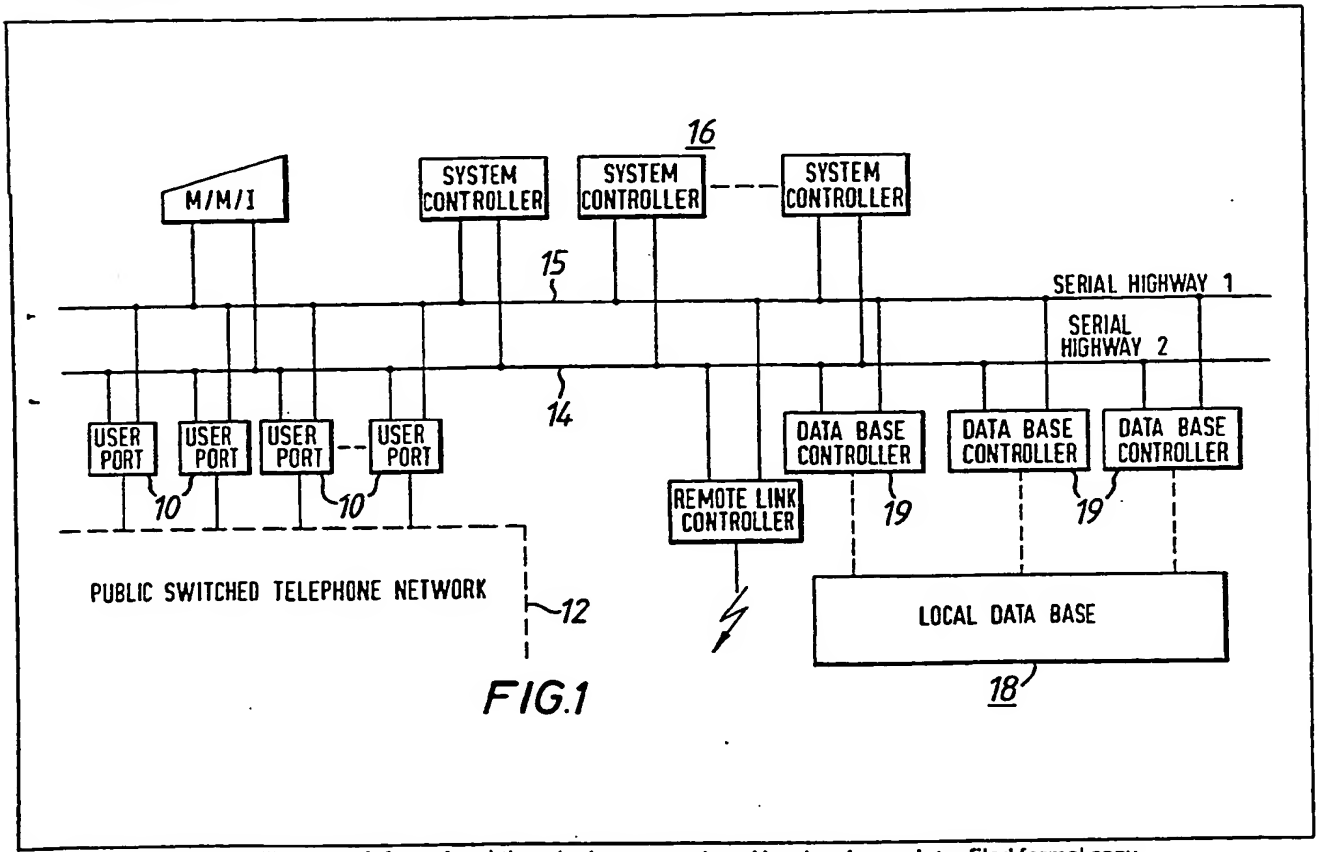

FIG.1

The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

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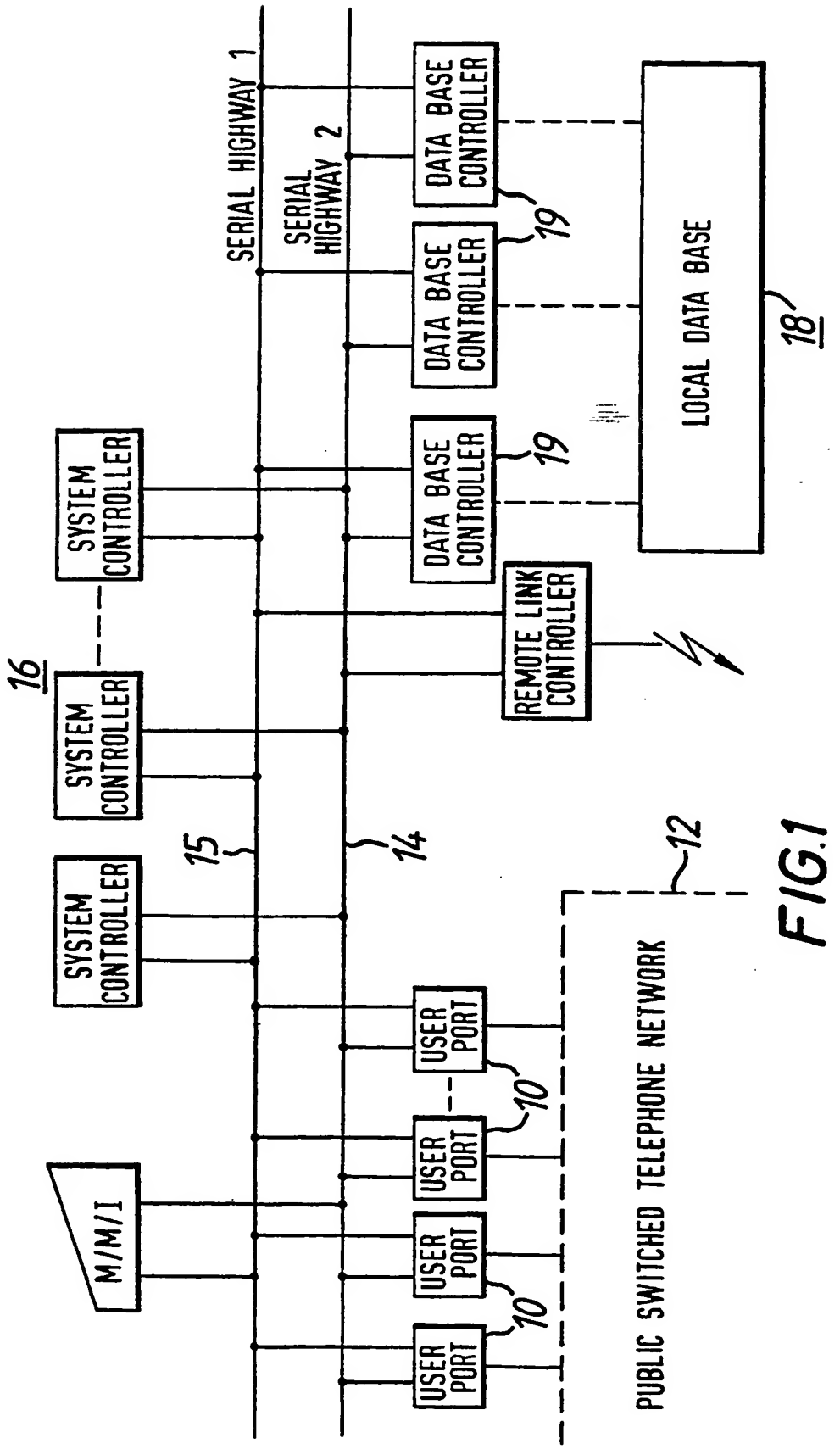

FIG.1

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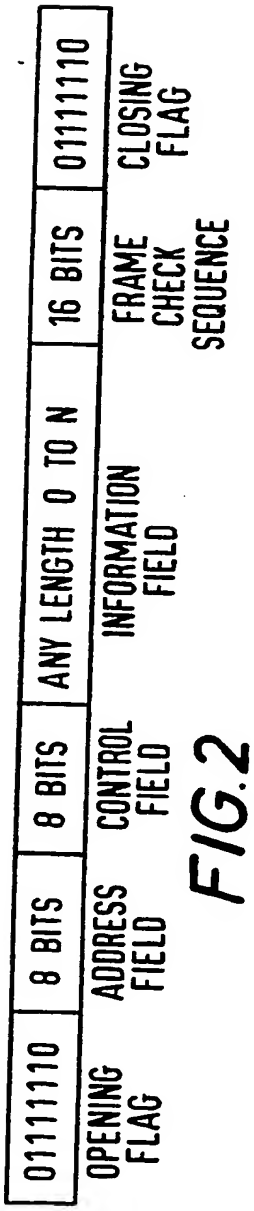

FIG.2

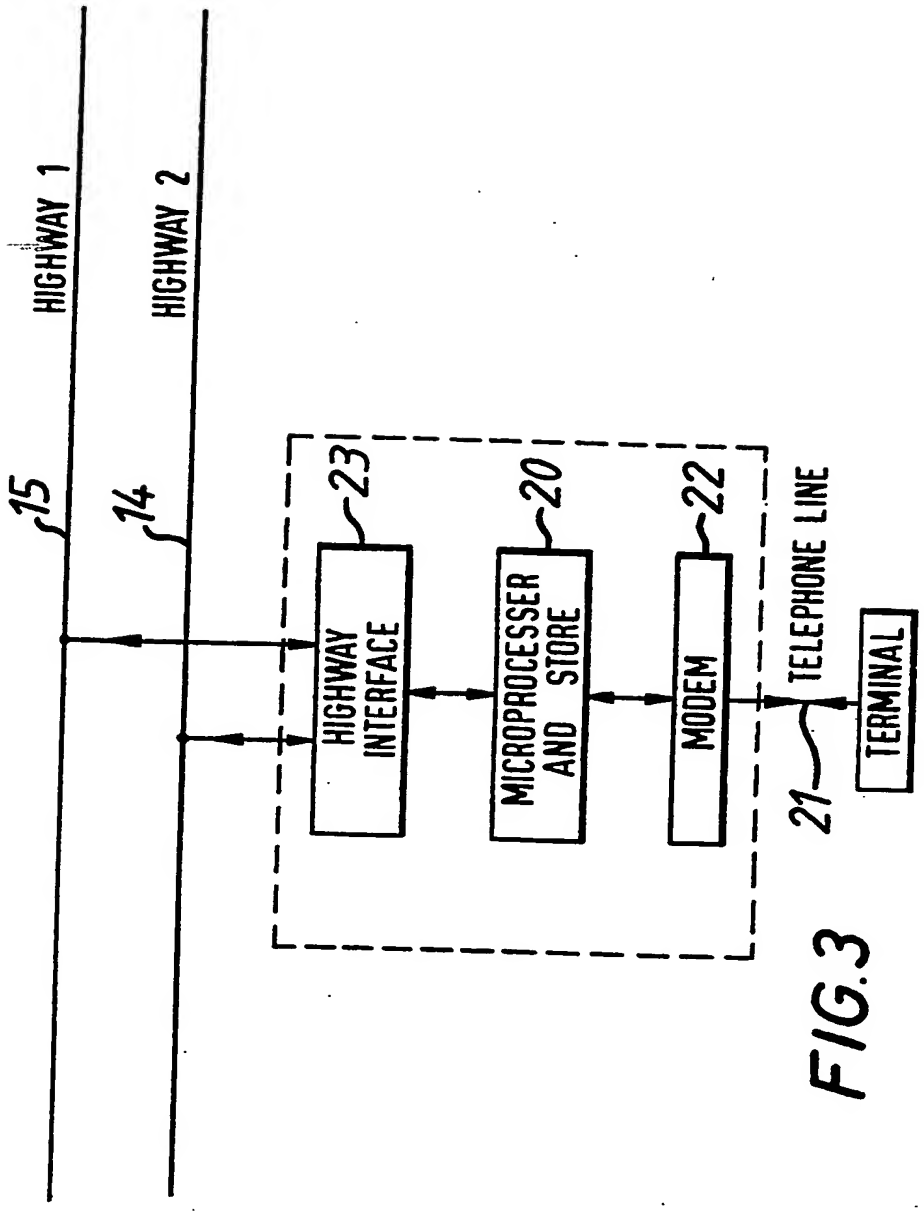

FIG.3

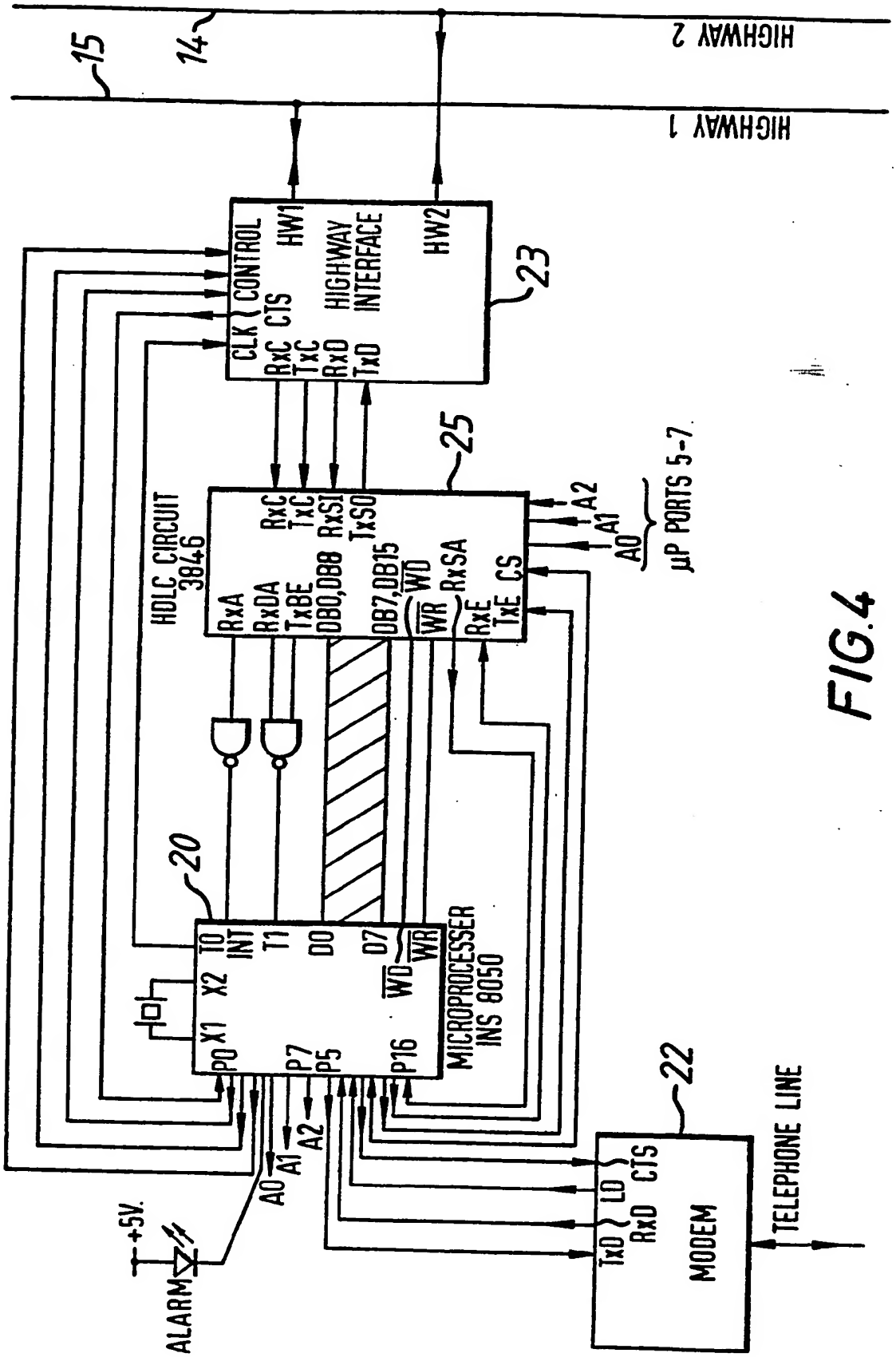

FIG.4

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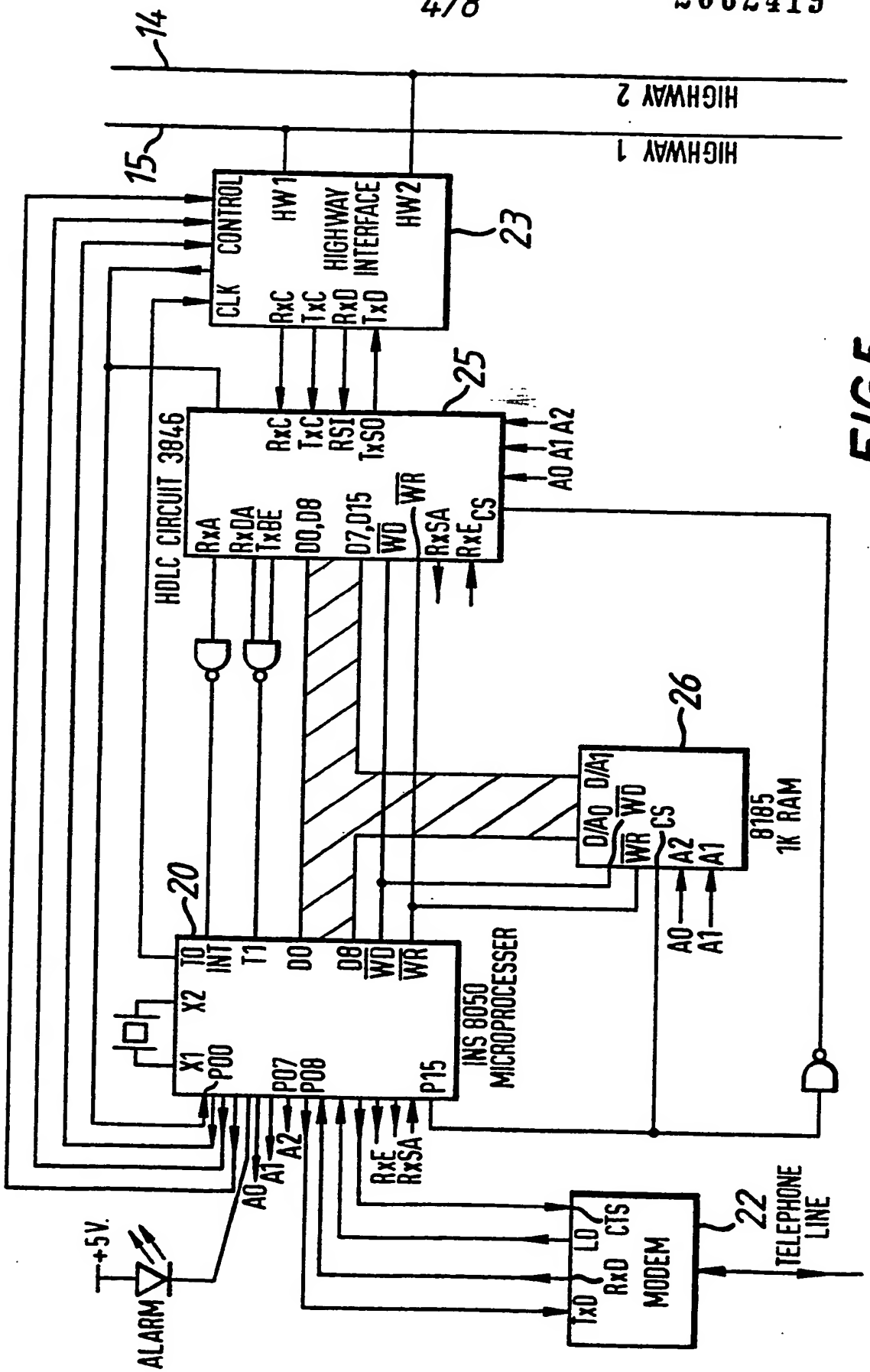


FIG.5

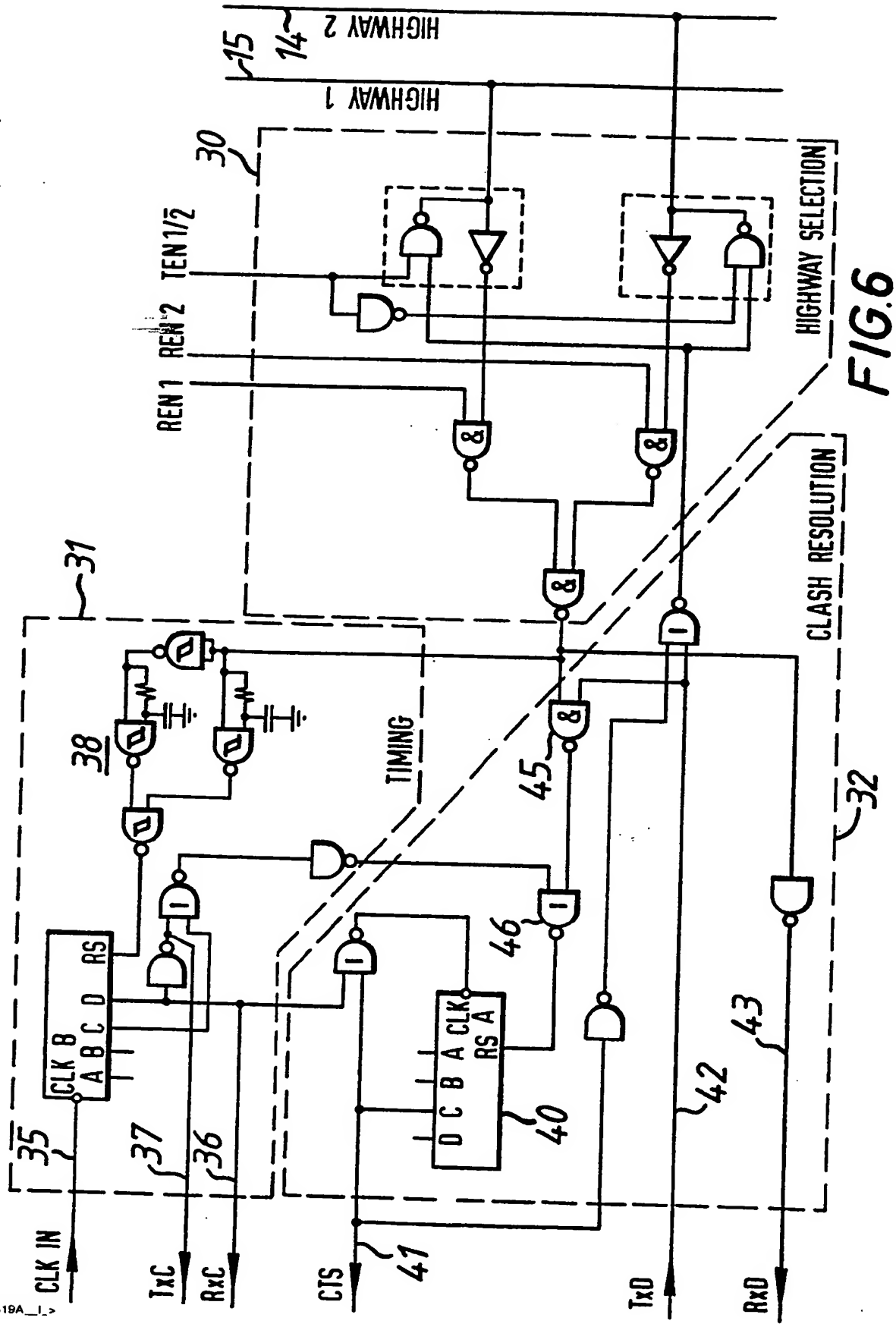
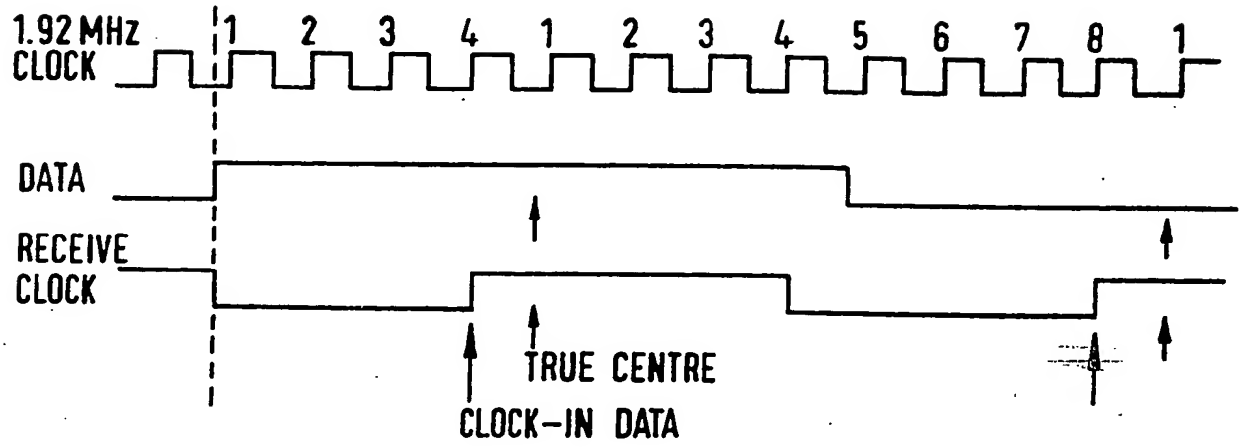
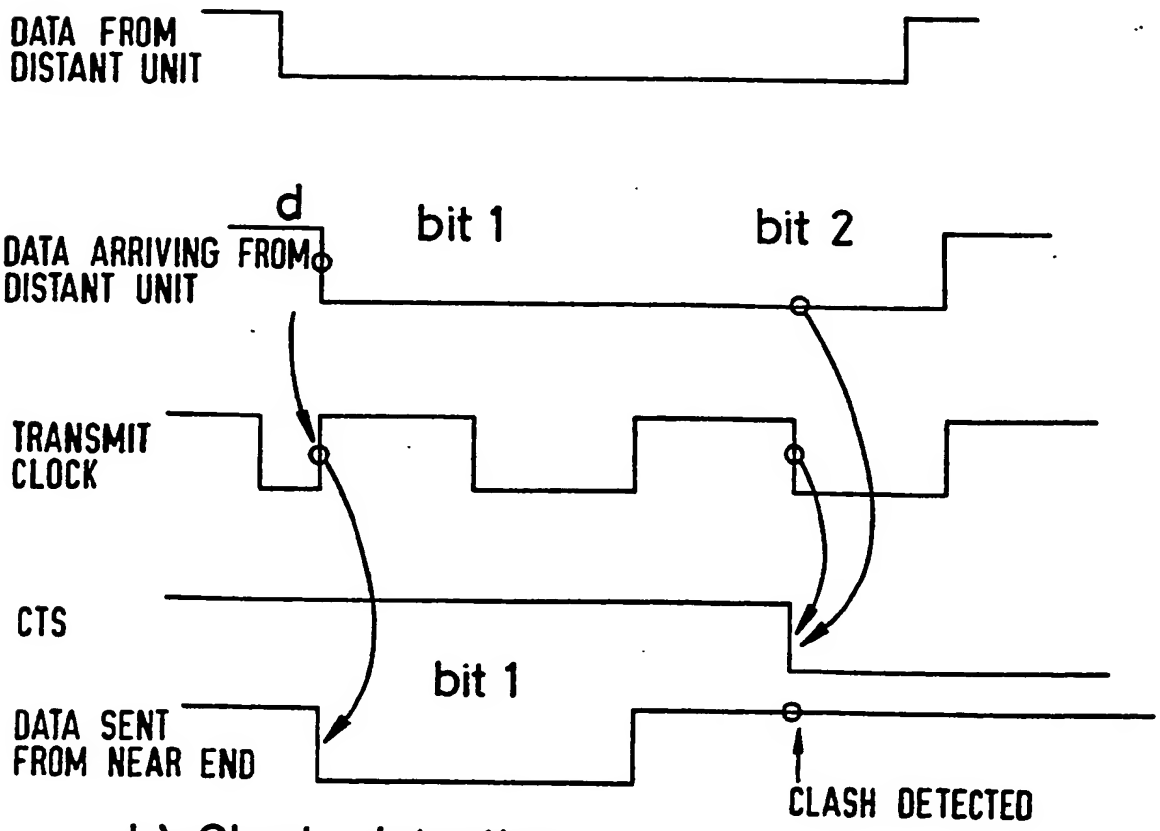


FIG.6

FIG.7



a) Synchronisation of the receive clock to the data.



b) Clash detection.

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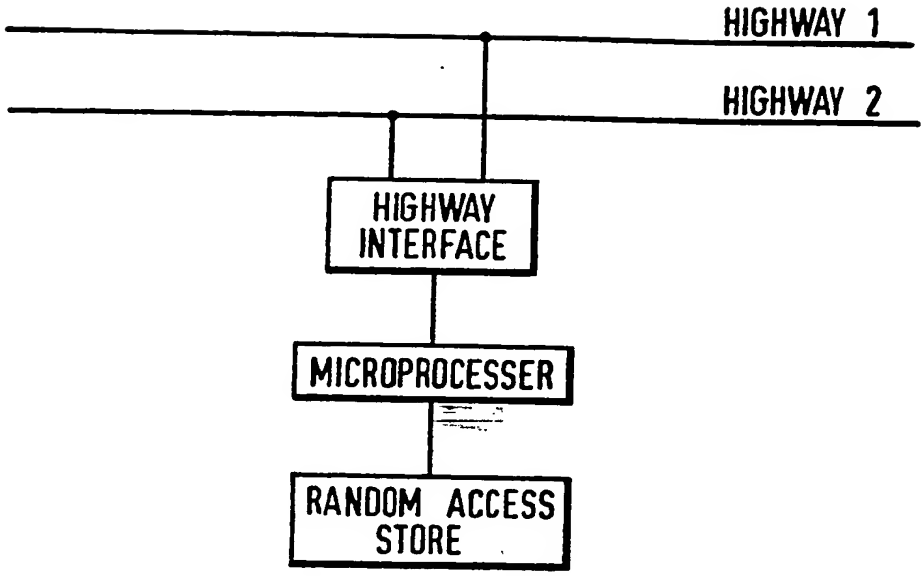

FIG.8

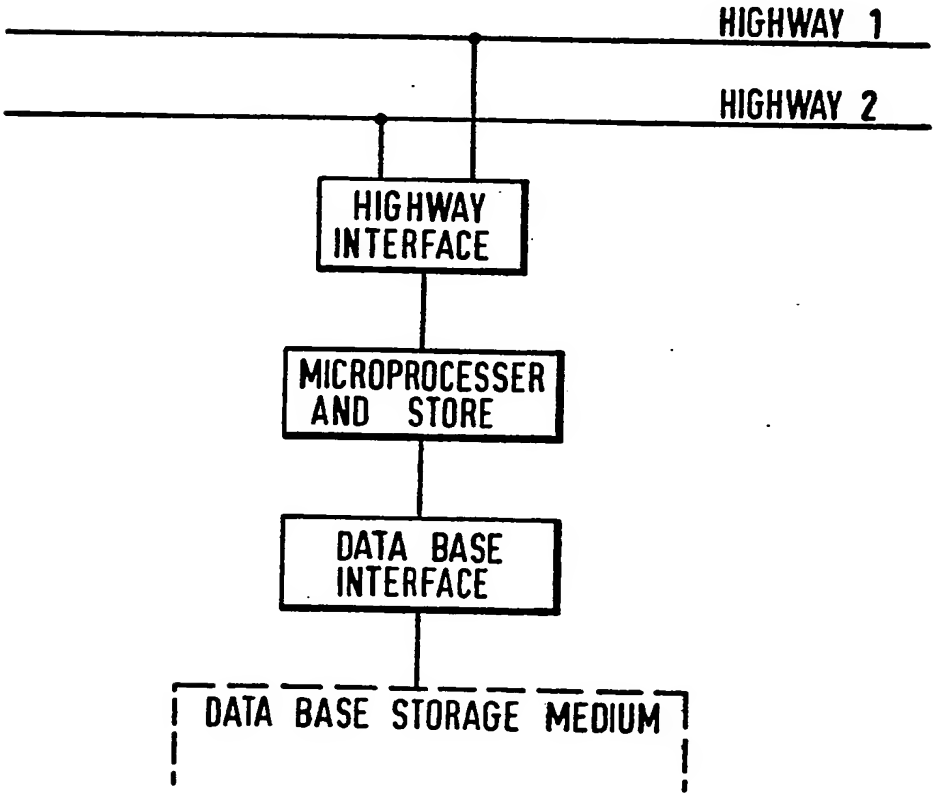

FIG.9

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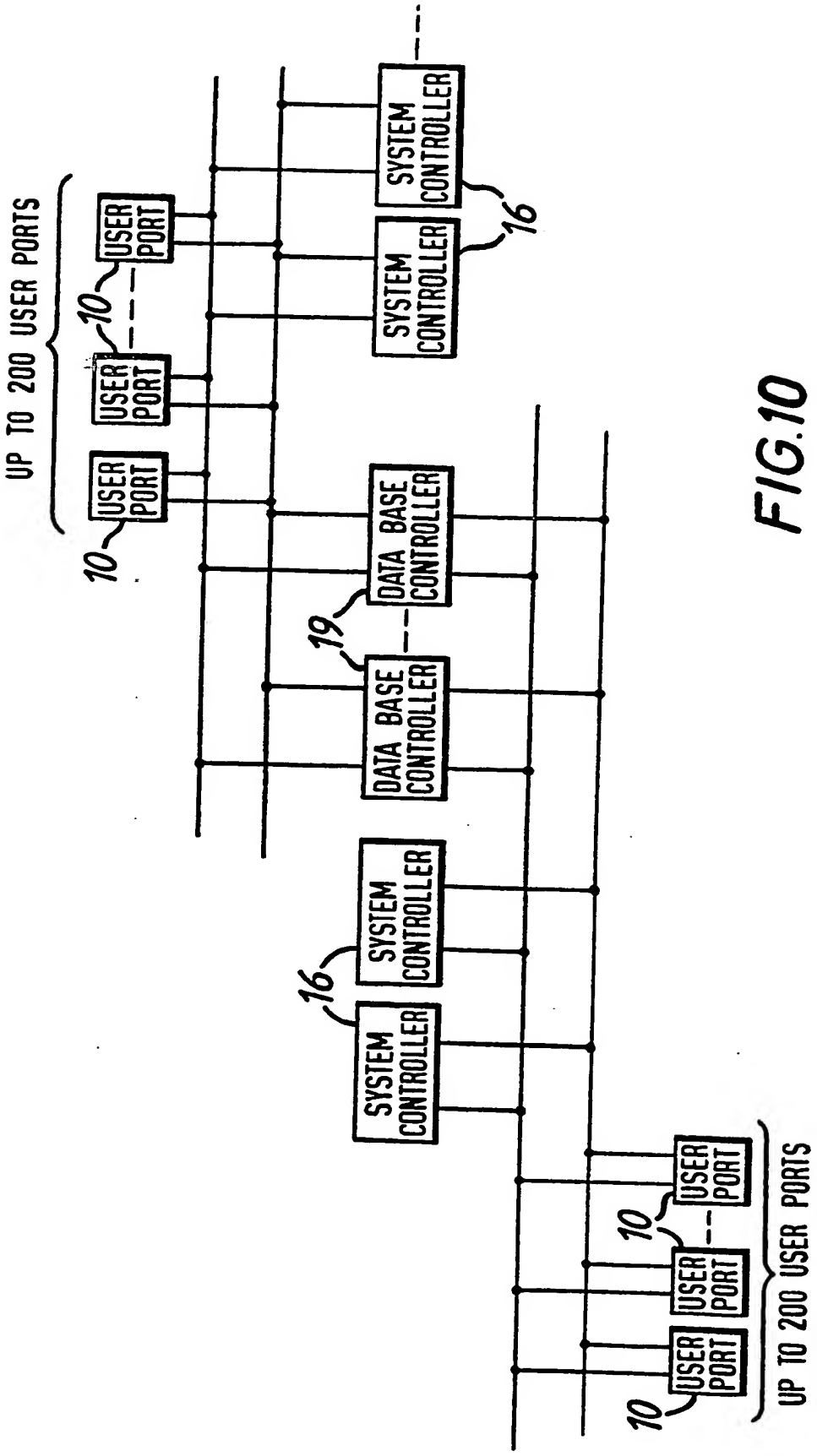

FIG.10

SPECIFICATION

Improvements in or r lating to information retrieval

This invention relates to apparatus for controlling communication between a data-base and a plurality of ports and in particular relates to such apparatus which can be implemented as a small viewdata centre.

Viewdata is an interactive information retrieval system which is based on a tree-ordered data-base accessed through a simple user protocol. The data-base is held in a computer and a user can gain access to the data via a telephone line. The information is transmitted from the computer centre to a viewdata terminal at a user's premises via the telephone line link and is displayed on a display unit such as a television screen.

A connected is made between a viewdata terminal and the computer centre by dialling the telephone number of the viewdata centre as for a normal telephone call. Once a connection has been established the user can gain access to the information he wants. At the highest level of the tree-ordered data-base the user is presented with a number of very general choices. By keying a single digit he can select one of these topics and will be presented with a further set of choices of a more specialised nature. This process is repeated until the required information is located.

Viewdata centres which exist at present have been designed to give a large number of users access to a substantial data-base. They are based upon a large central computing system of a secure pair of processors and are expensive. There are situations where smaller viewdata centres could provide a useful service. One application for a small viewdata centre is as a standalone viewdata service which could be used, for example, by a business organisation. It would provide an easily accessible data-base for various parts of an organisation or it could be used to provide a specialised enquiry service for members of the public. An advantage of a small data-base is that it is easier to update.

Another application for a small viewdata centre would be to provide a service for a small community concentrating on information of local interest. A further application is as a concentrator for a national viewdata system.

The present invention has arisen from a study of the design of a small viewdata centre although it is not limited to that application.

According to the present invention there is provided apparatus for controlling communication between a data-base and a plurality of ports, said apparatus comprising a plurality of first interface circuits each for connection to a port, a pair of serial highways, each interface circuit being connected to both serial highways, and at least one control unit for controlling communication between said first interface units and at least one second interface circuit associated with said data-base via said serial highways, said interface circuits including means for transmitting signals along said serial highways in a high-level data link c ntrol protocol.

Each first interface circuit may include a microprocessor, a high-level data link control protocol circuit connected to said microprocessor, and a highway interface connecting the high-level data link control protocol circuit to the serial highways.

Each highway interface may include a circuit for sensing data on said highways the arrangement being such that if said sensing circuit senses a "0" on a highway while the interface circuit is transmitting a "1", that interface circuit is caused to cease transmission. This arrangement is provided to resolve clashes due to two or more interface circuits attempting to start transmitting at the same time.

When the apparatus is in the form of a small viewdata centre the microprocessor of each first interface circuit is linked to a telephone line by a modem.

The invention will be described now by way of example only with particular reference to the accompanying drawings. In the drawings:

Figure 1 is a block schematic diagram of a small viewdata centre;

Figure 2 illustrates the frame format of synchronous data link control protocol;

Figure 3 is a block schematic diagram of a user port of the viewdata centre;

Figure 4 is a circuit diagram showing one form of user port;

Figure 5 is a circuit diagram showing another form of user port;

Figure 6 is a circuit diagram showing a highway interface circuit;

Figure 7 is a waveform diagram illustrating the operation of the clash resolution part of the highway interface circuit;

Figure 8 is a block schematic diagram of a system controller;

Figure 9 is a block schematic diagram of a data base controller, and

Figure 10 is a block schematic diagram of an expanded viewdata centre.

The present description relates to a small viewdata centre. The centre has been designed to operate with between ten and two hundred simultaneous users and makes use of fault tolerant computing techniques. The centre is shown schematically in Figure 1.

Referring to Figure 1 the centre has a plurality of user ports 10 each of which is arranged to provide an interface between the public switched telephone network indicated generally at 12 and a pair of serial highways 14, 15. System controllers 16 control communication between the user ports 10 and a data-base 18 via the serial highways 14, 15. The data-base 18 is linked to the highways 14, 15 by data-base controllers 19.

The local data-base contains pages of information which are relevant to the particular users who are linked to the centre by the public switch telephone network. Users can access the local data-base via the user ports under the

control of the system controllers and appropriate pages of information are transmitted from the data-base over the telephone network.

The viewdata centre has been designed to operate with a transmission sp ed on the highways 14, 15 of the order of 200 Kbits per sec nd. The transmission scheme is based on a high level data link control (HDLC) protocol to give bit and frame synchronisation and a fixed protocol for the formation of messages. In particular it is proposed to use a synchronous data link control (SDLC) protocol the frame format of which is illustrated in Figure 2 of the drawings. The boundaries of a frame are indicated by opening and closing flags. A receiver hunts for this pattern on a bit by bit basis to determine the start of a frame. Any data occurring between two flags is considered to be a frame of information and the various fields are interpreted accordingly. The first field in the frame holds the destination address for the frame. This is followed by a control field for special information about the nature of the frame and how it should be processed. Next comes the data portion of the frame and when all the data has been transmitted the frame is terminated by a frame check sequence. This is a cyclic redundancy code generating using a known polynomial. The frame is completed by sending a closing flag and the transmitter can then send the next frame, send flag characters to maintain synchronisation or simply remain idle.

Synchronous data link control protocols are well known and documented. A number of commercial integrated circuits are available for this type of operation and most of these are designed to interface directly with microprocessor systems.

The centre also incorporates a technique for controlling access to the highways from the user ports in the event of a clash. This technique will be described in detail with reference to the user ports.

In the present design it will be noted that dual serial highways are arranged to link the user ports and data base. This design has been chosen to reduce the likelihood of a single fault effecting the whole system.

The formation of packets or messages in the centre of Figure 1 is defined by the SDLC type protocol adopted for the communication links, but the type of message required and the use to which they are put is a function of the system design.

The basic cycle of events in the centre can be defined as follows:—

a) A user interacts with the terminal and a character is sent to the viewdata centre.

b) The user port 10 receives the character and forwards its new state to the system controllers 16.

c) One of the controllers 16 decides on any action required and forwards a request to the data-base 18 for a new frame if necessary.

d) If the data-base 18 is called on it will find the requested frame and transfer it to the user port 10 ready for transmission to the customer.

Any viewdata call can be considered to be made up from a number of such cycles although the interactions at the beginning and ending of the call may be slightly more complex. The various messages required to complete that cycle can be defined as follows:—

a) User port 10 to system controller 16.

When a user port 10 receives a character over the line from the customer it does not attempt to interpret it but immediately sends a message to a system controller 16. This message contains all the information that the controller needs to interpret the character, including details such as previous digits keyed, previous frame sent, state of user port, etc. This data is held in a dedicated block of storage in a microprocessor in the user port and is transmitted with every message. The total message is about 32 words long. It is addressed to any of the controllers and those that are free receive the message and begin to respond to it. The first controller to seize the highway (by chance) sends an acknowledgement (ACK) message to the user port and the others, seeing this message on the highway, cancel their own acknowledgement and return to an idle condition awaiting another request. If the user port microprocessor does not receive an acknowledgement within a given time, possibly because the original message was corrupted, there were no free controllers at the time, or even that the acknowledgement itself was lost, it will retransmit the original message. If the reason for failure was the loss of the first message, repeating the message could lead to a repeated reply. This should not cause any problem since the second reply, whether from the controller or the data-base, will be identical to the first and will simply overwrite it before the microprocessor in the user port has started to take very much action. If the multiple reply is a problem, each originating message could be given a code which would be incorporated in the reply so that the receiver could differentiate between them.

b) Controller to user port.

Acknowledgement messages sent from the controller to the microprocessor in the user port on receipt of a request are sent as quickly as possible so that the 'unsuccessful' controllers are released without delay. However, after processing the request further, the controller may wish to update the state of the microprocessor in the user port. It does this by sending a message incorporating a copy of the data area that holds the microprocessor status with the appropriate changes made. This will update the microprocessor in the user port so that the next request it makes contains all the relevant data. The controller will expect an acknowledgement to the message and if one is not received in a given time it will retransmit. Again, if the acknowledgement is lost the microprocessor in the user port will receive the update twice, but this should not cause any problem.

c) Controller to data-base controller.

When the character received by the

microprocessor in the controller 16 indicates that a new frame is required, the full identification of the frame is determined by the controller which prepares a message for the data-base controller 19. This message contains the identity of the microprocessor in the user port so that the frame can be sent directly to it. Depending on the arrangement of the data-base, the system controller 16 either sends the message direct to one particular data-base controller or else to a group of controllers. In either case, it will expect an acknowledgement and will retransmit if necessary.

d) Data-base controller to user port.

The data-base controller obtains the frame of information requested by the system controller and prepares to transmit it to the user port. The size of each packet used for transmission depends on a number of factors. The maximum size of packet is governed partly by the error rate of the channel. As the size of packet is increased the probability of an error is increased and the cost of retransmission also increases. With an average error rate of 1 in 10^5, the fraction of packets requiring retransmission is about 1% for packets of 128 words. The maximum size is also affected by the size of the buffer on each microprocessor. If it is kept small then the hardware may be made very simple, but this may require multiple requests to the data-base for each frame which could be extremely inefficient. The minimum size of packet is governed by the need for efficient transmission and each separate packet requires overheads both in transmission and in processing. Messages from the data-base to the user port require acknowledgements but if a single frame consists of a number of packets sent closely following one another it may be possible to acknowledge the complete frame and only request retransmission of those packets received with errors.

Referring now to Figure 3 of the drawings there is shown schematically a user port 10. The user port 10 comprises a microprocessor and associated store 20 which is linked to a telephone line 21 by a modem 22 and to the highways 14, 15 by a highway interface circuit 23. The highway interface circuit 23 includes a high level data link control protocol circuit.

The user port which forms the interface between the telephone line 21 and the rest of the viewdata centre has two main functions. One is to accept data from the telephone line (d.c. line conditions and characters sent via the modem 22) and to forward these along with details of the current state of the connection to one of the system controllers 16. The other main function is to accept frames of information sent over the highways 14, 15 from the data-base and to transmit these to the customer over the telephone line 21 at a slower rate. It must also be able to accept other messages from the controller 16 and to be able to perform diagnosis routines on itself and on the highways.

A suitable microprocessor for use in the user port is an Intel INS 8050 and a design based on this microprocessor is shown in Figure 4 of the drawings. This microprocessor has sufficient storage to buffer a message of 128 bytes and still leave enough memory for general use by the microprocessor.

A number of integrated circuits are now available which will support an HDLC protocol on the serial highways and interface with the microprocessor. In the main all are designed for direct connection to a microprocessor and communication between the microprocessor and the HDLC circuit is usually by way of addressable registers on the HDLC circuit or by dedicated status pins. Some of the registers are used to control various options available while others are used for the transfer of data to and from the serial highways and to communicate the state of the circuit. Data to be sent out is transferred to a transmit data register and is converted to serial form. The HDLC circuit opens each message with a flag and when the microprocessor indicates that the last word of the message has been transferred it terminates the message with a framed check sequence and a closing flag. On the receive side the HDLC circuit indicates to the microprocessor that a message is being received and makes data available as it arrives. When the closing flag has been received it checks the frame check sequence and gives an indication if the frame has been received correctly or not. In the circuit shown in Figure 4 the HDLC circuit is a Fairchild F3846 circuit indicated at 25.

In the circuit shown in Figure 4 the microprocessor 20 has two 8 bit ports which can be used for general input and output. Any of the pins can be used as either an input or a latched output. The pins are used for various control functions on the user port including control of th telephone and highway interfaces providing addresses for the HDLC circuit 25 and for providing alarm indications. A third 8 bit port can be used for input and output or used to interface with external memory or peripheral units. It will be noted that there is a direct connection between the microprocessor and modem 22 since the type of microprocessor used is fast enough to handle the information itself using software. This means that if sufficient RAM is used on the microprocessor the only component needed to be connected to the bus is the HDLC circuit.

If necessary an external 1 Kbit RAM may be incorporated and an arrangement with such a memory is shown in Figure 5 of the drawings. The RAM is shown at 26 in this Figure. In this case switching between the HDLC circuit and the memory is performed using one bit on the input/output port.

The microprocessor has some other input/output lines which are used in the user port f r special purposes. The T0 pin can act as either an input or an output. As an input its condition can be tested using a single instruction and as an output it can be used to give a clock utput that is one third of the microprocessor crystal frequency. In the user port it is used as an output and the

clock frequency is used as a basis for the generation of cl cks for the HDLC circuit. The T1 pin is also testable using a single instruction and it is used to test the receiver data available and the transmitter buffer empty to enable data transfers to and from the HDLC circuit to be made as quickly as possible. The interupt is an input which forces the microprocessor to jump to a particular area of program. It is used to indicate that a message is arriving and forces the microprocessor to service it.

The clock frequency used in the user port is 5.76 MHz. This is high enough to allow two hundred user ports to be connected to the highways 14, 15 and it is also slow enough for the microprocessor to handle each bit as it arrives.

The highway interface circuit 23 as shown in Figures 3, 4 and 5 is illustrated in more detail in Figure 6. The highway interface circuit has three main sections indicated at 30, 31 and 32. The section 30 provides gating to the two highways 14, 15 and comprises a number of gates interconnected as shown. These gates are driven by separate output pins from the microprocessor and are arranged to give it full control over received data. The arrangement is such that under normal operation the user port can monitor data appearing on both highways 14 and 15 but if one highway becomes faulty the circuit can isolate it and only receive data from that highway which is functioning correctly. The user port like other units, only transmits on one highway at a time but gates are provided so that the one used is under processor control.

The clock generation section 31 receives a clock signal from the T0 pin of the microprocessor on line 35 and generates a receive clock on line 36 and a transmit clock signal on line 37. The input on line 35 is 1.92 MHz and this is divided by 8 to give 240 KHz. The transmit clock can be free running but the receive clock is synchronised to incoming data. Gates 38 form a differentiating circuit which produces a short pulse each time a transition occurs in the data. This resets the dividing circuit and exactly four clock periods later a positive transition occurs on the line 36. Providing that a reset occurred at the true beginning of the bit period, the positive transition on line 36 occurs in the middle of the bit period and clocks the data into the HDLC circuit. Fuirther positive transitions continue to occur on the line 36 every eight clock periods in the middle of each bit period and they are re-synchronised with every transition in the data. It is a feature of HDLC protocol with non-return to zero coding that these occur at least every 5 bits so with crystal control clocks there is no danger of the receive clock drifting out of syncronisation.

The section 32 is a clash resolution section which is operative to control access to the highways 14, 15 in the event that several user ports try to gain access at the same time. Each user port must be able to detect when a highway is free and if, when it is transmitting, a clash occurs it must stop and wait for the highway to become free again. The simplest way to detect activity on a highway is to monitor the occurrence of "0's". With non-return to zero coding "0's" occur at least once in every six bits during a message, or possibly after seven bits in a flag. When the line is idle it will be in a "1" condition so eight successive "1's" indicate that it has just become idle. In the arrangement shown in Figure 6 this situation is detected using a counter 40 which is reset by every "0" on the line but give a clear to send signal on line 41 when it has counted up to eight consecutive "1's". A clash is indicated by a unit transmitting "1" on line 42 and the receiver detecting a "0" on line 43. When this happens the counter 40 is reset via the gates 45 and 46, thus removing the signal on line 41 and disabling any further data transmission until the highway is free again. However, if the unit is transmitting a "0" itself this is seen by the detector and the signal on line 41 is not removed. The logic is arranged to provide this.

In the present system the highway is sampled once every bit period. It can be shown that because of the way in which the clocks are synchronised to the incoming data and because the maximum transmission delay is small in comparison with the bit period of 4 μ sec when two user ports do try to gain access to the highways together their data is almost exactly synchronised. While they transmit the same data bits neither will be able to tell that the other is transmitting but as soon as they differ, the unit sending the "1" sees a "0" and withdraws. The other unit continues transmitting and no data is lost. The fact that one unit is always successful in accessing the highway means that highway utilisation can be very high.

Wavefroms indicating clash detection are shown in Figure 7 of the drawings.

Referring now to Figure 8 of the drawings each system controller 16 comprises a microprocessor 50 which can communicate with other units over the highways 14, 15 via a highway interface circuit 51. The microprocessor can be an 8085 microprocessor which is widely used in the telecommunications field. This microprocessor requires a large random access memory which is indicated at 52. This can be provided by a small number of integrated circuit such as those of type 8185 which are directly compatible with an 8085 microprocessor. The system controller operates generally as a conventionl microprocessor apart from the highway interface 51 which is similar to that provided in each user port 10.

A block diagram of a data-base controller 19 is given in Figure 9. Each data-base controller comprises a microprocessor and store 60 which is linked to the highways 14, 15 by a highway interface circuit 61. The microprocessor 60 and its associated store is linked t the data base storage medium 63 by a data base interface circuit 64. The highway interface 61 is similar to that used in the user ports 10 and the system controllers 16. The microprocessor arrangement 60 is based on a 8085 microprocessor and the data base interface

64 is designed to permit access to different storage devices. Most data bas interfaces require direct memory access to enable data to be transferred rapidly enough. A direct memory access circuit which can be used is type 8257. This has a number of direct memory access channels so one of the others could be used to simplify transfers to the HDLC circuit.

The data base controllers may be arranged so that a number have access to the same information or so that each has its own dedicated area. Ideally the data-base should hold the details of its own structure. The system controllers can then address request for data to the data base controllers as a group and then the particular controller actually answering the request could either provide the information itself or else direct the request to the correct one. In the case of a data-base held on a number of disc units each disc would hold copies of the most frequently accessed frames along with its own specialised frames and information about where the other frames are held.

If the system is connected to a large viewdata network it would require other data-base controllers with links to remote computer centres. These links could be ordinary data links with data rates of up to 9 K baud or special circuit or packet switched links operating at 48 K baud.

The centre described above is designed to have an upper limit of two hundred user ports. This is limited by the speed of the highways and the addressing capabilities of the system which is simplified considerably if the number of units on one highway is less than 256. However, the system could be expanded by combining a number of highway systems and giving them access to a common group of data-base controllers. The ultimate size of the system is then only limited by the speed of the message switches which combine the highways and the number of requests that the data-base controllers can handle. A possible structure for an expanded system is shown in Figure 10.

The principle of the 'memoryless marker' has been advocated for use in electronic telephone exchanges. The use of highways of the type designed for the centre described above could provide a suitable basis for incorporating this principle by linking the peripheral units in a telephone exchange (e.g. line units and signalling units) to a group of controllers. The various tasks required in the processing of a call could be distributed between different groups of controllers (e.g. some for setting up paths, others for number and routing translations, etc.) and there would then be no need for a central computer system.

CLAIMS

1. Apparatus for controlling communication between a data-base and a plurality of ports, said apparatus comprising a plurality of first interface circuits each for connection to a port, a pair of serial highways, each interface circuit being connected to both serial highways, and at least one control unit for controlling communication between said first interface units and at least one second interface circuit associated with said data-base via said serial highways, said interface circuits including means for transmitting signals along said serial highways in a high-level data link control protocol.

2. Apparatus as claimed in claim 1 wherein each first interface circuit includes a microprocessor, a high level data link control protocol circuit connected to said microprocessor, and a highway interface connecting the high-level data link control protocol circuit to the serial highways.

3. Apparatus as claimed in claim 1 or claim 2 wherein each highway interface includes a circuit for sensing data on said highways the arrangement being such that if said sensing circuit senses a "0" on a highway while the interface circuit is transmitting a "1", that interface circuit is caused to cease transmission.

4. Apparatus as claimed in claim 2 or claim 3 wherein the apparatus is in the form of a small viewdata centre and the microprocessor of each first interface circuit is linked to a telephone line by a modem.

5. Apparatus substantially as hereinbefore described with reference to and as shown in the accompanying drawings.

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